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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,648	08/13/2001	Thomas H. Lee	035905/0104	6565

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EXAMINER	
WEISS, HOWARD	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,648	Applicant(s) LEE ET AL.	
	Examiner Howard Weiss	Art Unit 2814	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *99-105,450,456-466 and 475-507* is/are pending in the application.

4a) Of the above claim(s) *499-507* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *99-105,450,456-466 and 475-498* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Attorney's Docket Number: 035905/0104

Filing Date: 8/13/01

Continuing Data: CIP of 09/801,233 (03/06/01) which is a CIP of 09/745,125 (12/21/00) which is a CIP of 09/639,579 (8/14/00) which is a CIP of 09/639,702 (8/14/00) which is a CIP of 09/639,749 (8/17/00) which claims benefit of 60/279,855 (3/28/01)

Claimed Foreign Priority Date: none

Applicant(s): Lee et al. (Subramanian, Cleeves, Walker, Petti, Kouznetzov, Johnson, Farmwald, Herner)

Examiner: Howard Weiss

Election/Restrictions

1. Newly submitted Claims 499 to 507 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

I. Claims 99 to 105, 450 and 456 to 498, drawn to semiconductor device, classified in Class 257, Subclass 296;

II. Claims 499 to 507, drawn to a process for making a semiconductor device, classified in Class 438, Subclass 14+.

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention, since the Group I invention could be made by planarizing between the device levels using etchback techniques instead of CMP (Claim 499).

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, Claims 499 to 507 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Initially, and with respect to Claims 99, 101, 450, 456, 462 to 464, 479, 480, 491 and 498, note that a "product by process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al., 227 USPQ 964 (CAFC, 1985)* and the related case law cited therein which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

> even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); Buono v. Yankee Maid Dress Corp., 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).*

Note that Applicant has burden of proof in such cases as the above case law makes clear.

4. Claims 450, 456, 489 and 491 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe (U.S. Patent No. 5,091,762)and Uochi et al. (U.S. Patent No. 6,028,326).

Watanabe shows most aspects of the instant invention (e.g. Figures 6) including a monolithic 3-D array of charge storage devices **77** with a plurality of substantially planarized device levels **80**.

Watanabe does not show the first layer of transition metal-crystallized silicon and the array of polycrystalline or amorphous material. Uochi et al. teach (e.g. Figures 1) to use a layer of amorphous silicon and to transform part of said layer to polycrystalline transition metal-crystallized silicon **12a** to produce a device with high mobility at low temperatures and shorter times (Column 1 Line 44 to Column 2 Line 45). It would have been obvious to a person of ordinary skill in the art at the time of invention to use a layer of transition metal-crystallized silicon as taught by Uochi et al. in the device of Watanabe to produce a device with high mobility at low temperatures and shorter times.

As to the grounds of rejection under section 103(a), how the device levels are planarized (either by CMP or some other means) and how the layers are deposited (either in a monolithic fashion or separately and then packaged together) pertains to

intermediate process steps and does not affect the final device structure. See MPEP § 2113 which discusses the handling of "product by process" claims.

5. Claims 457 to 463, 465, 466, 489 to 491 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe and Uochi, as applied to Claim 456 above, and in further view of Zhang (U.S. Patent No. 5,835,396).

Watanabe and Uochi show most aspects of the instant invention (Paragraph 4) except for the array containing four or more levels and the change storage device comprising a pillar diode, a pillar TFT EEPROM, a self aligned TFT EEPROM or a rail stack TFT EEPROM. Zhang teaches (e.g. Figure 15A) to have a device with 4 or more levels **500a-d** to produce a device with high memory density (Column 2 Lines 1 to 19). It would have been obvious to a person of ordinary skill in the art at the time of invention to have a device with 4 or more levels as taught by Zhang in the device of Watanabe and Uochi to produce a device with high memory density. In reference to the change storage device comprising a pillar diode, a pillar TFT EEPROM, a self aligned TFT EEPROM or a rail stack TFT EEPROM, Watanabe states (Column 2 Lines 51 to 53) that the invention is applicable to any type of memory device. This would encompass all the memory devices of the instant invention.

6. Claims 464, 475 to 482 and 492 to 498 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe, Uochi and Zhang, as applied to Claim 456 above, and in further view of Kub (U.S. Patent No. 6,153,495).

Watanabe, Uochi and Zhang show most aspects of the instant invention (Paragraph 5) except for the roughness being less than 4000 Angstroms. Kub teaches (Column 6 Lines 3 to 7) to have a roughness less than 4000 Angstroms for direct bonding of substrates together. It would have been obvious to a person of ordinary skill in the art at the time of invention to have a roughness less than 4000 Angstroms as taught

by Kub in the device of Watanabe, Uochi and Zhang for direct bonding of substrates together.

7. Claims 99 to 101 and 483 to 488 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe and Uochi, as applied to Claim 456 above, and in further view of Matsushita (U.S. Patent No. 5,998,808).

   Watanabe and Uochi shows most aspects of the instant invention (Paragraph 4) except for the monocrystalline semiconductor substrate. Matsushita teaches (e.g. Figure 1) to use a monocrystalline semiconductor substrate **101** to realize 3-D integrated circuit devices (Column 1 Lines 34 to 51). It would have been obvious to a person of ordinary skill in the art at the time of invention to use a monocrystalline semiconductor substrate as taught by Matsushita in the device of Watanabe and Uochi to realize 3-D integrated circuit devices.

8. Claims 102 to 105 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe, Uochi and Matsushita, as applied to Claim 99 above, and in further view of Zhang.

   Watanabe, Uochi and Matsushita show most aspects of the instant invention (Paragraph 7) except for the array containing four or more levels and the change storage device comprising a pillar diode, a pillar TFT EEPROM, a self aligned TFT EEPROM or a rail stack TFT EEPROM. Zhang teaches (e.g. Figure 15A) to have a device with 4 or more levels **500a-d** to produce a device with high memory density (Column 2 Lines 1 to 19). It would have been obvious to a person of ordinary skill in the art at the time of invention to have a device with 4 or more levels as taught by Zhang in the device of Watanabe, Uochi and Matsushita to produce a device with high memory density. In reference to the change storage device comprising a pillar diode, a pillar TFT EEPROM, a self aligned TFT EEPROM or a rail stack TFT EEPROM, Watanabe states (Column 2 Lines 51 to53) that the invention is

applicable to any type o memory device. This would encompass all the memory devices of the instant invention.

Response to Arguments

9. Applicant's arguments filed 8/6/03 have been fully considered but they are not persuasive. In reference to Watanabe teaching the use of epitaxial silicon, it is evident from the wording used ("When a vapor phase epitaxial method is used ...") that it is a suggested method and not essential to the invention of Watanabe. Disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments. *In re Susi, 440 F.2d 442, 169 USPQ 423 (CCPA 1971).* "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." *In re Gurley, 27 F.3d 551, 554, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994).* The Applicants are correct that Watanbe does not specify the crystanallinaty of the layers. Uochi provides the reason to use polycrystalline and amorphous silicon.

In reference to the planar layers, the Applicants state that just because Watanabe shows planar layers and states that the layers are planar, it does not follow that the layer are highly or "substantially" planar. However, the Applicants are arguing degree not substance. The layers of Watanabe are substantially planar as opposed to being non-planar. "Highly or "substantially" are subjective degrees of planization and does not patently distinguish the instant invention from the prior art. Although a claim should be interpreted in light of the specification disclosure, it is generally considered improper to read limitations contained in the specification into the claims. See *In re Prater, 415 F.2d 1393, 162 USPQ 541 (CCPA 1969)* and *In re Winkhaus, 527 F.2d 637, 188 USPQ 129 (CCPA 1975)*, which discuss the premise that one cannot rely on the specification to impart limitations to the claim that are not recited in the claim. Other claims (e.g. Claim 475) actually quantify the degree of planarity.

In reference to the use of "monolithic", the Examiner is treating this limitation as a "product-by-process" limitation. How the device is assembled, either in a monolithic fashion or separately and then packaged together, pertains to intermediate process steps and does not distinguish the final prior art device structure from the instant invention. In view of these reasons and those set forth in the present office action, the rejections of the stated claims stand.

Conclusion

10. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **-7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications. The official TC2800 Before-Final, **(703) 872-9318,** and After-Final, **(703) 872-9319**, Fax numbers will provide the fax sender with an auto-reply fax verifying receipt of their fax by the USPTO.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(703) 308-4840** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via **Howard.Weiss@uspto.gov**.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 Receptionist at **(703) 308-0956**.

12. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/74, 296	thru 10/3/03
Other Documentation: none	
Electronic Database(s): EAST, IEL	thru 10/3/03

HW/hw
8 October 2003

Howard Weiss
Examiner
Art Unit 2814